A SI-CMOS-MEMS PROCESS USING BACK-SIDE GRINDING

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ABSTRACT

This paper presents a Si-CMOS-MEMS fabrication process which leaves the back-side silicon under the CMOS metal and oxide layers, and improves the uniformity of the back-side silicon using back-side grinding. The Si-CMOS-MEMS process includes a grinding process followed by a bonding process and conventional post-CMOS etch. A Si-CMOS-MEMS accelerometer is used to demonstrate the feasibility of the Si-CMOS-MEMS process. A 0.2 µm flatness of ground silicon surface over 2 mm length is achieved in this work. With this process, the measured sensitivity reaches 4.5 mV/g and ultra high flatness less than 0.05 µm out-of-plane variation of released accelerometers is achieved.

INTRODUCTION

Background

The CMOS-MEMS process [1] directly integrates MEMS structures and CMOS circuitry to reduce parasitic capacitance from wiring and to reduce packaging cost for future multi-device MEMS. However, thin film CMOS-MEMS devices have exhibited curling and nonuniform surfaces, especially for large MEMS devices such as micromirrors. For this reason, thick film CMOS-MEMS devices with high aspect ratio structures have been a major trend in some applications, such as inertial sensors, RF resonators and electrostatic actuators. This method yields superior flatness and high sensitivity based on a higher coefficient term in dC/dx in capacitive devices.

In previous work fabricating thick-film CMOS-MEMS devices, a DRIE-CMOS-MEMS process [2-3] was applied using a patterned back-side Si DRIE to form a 50 µm bulk Si structural layer. However, this method results in a high surface roughness on the back-side profile, which leads to variation in the device performance. This method also requires overetching in the front side Si DRIE release step. The ARDEM-CMOS-MEMS process, another previous work, [4] is a derivative that provides improved thickness variation (±2.5 µm) of the back-side profile. However, even this level of thickness variation can cause significant variation of the device's performance, while still requiring overetching in the front-side release step. Figure 1 compares the surface profile of the back-side silicon for these two processes with the proposed back-side grinding Si-CMOS-MEMS process. As the figure illustrates, precision grinding and polishing provide a superior thickness variation of 0.2 µm and the chip thickness varies within only 5 µm from die to die.

In this work, a recently published silicon-on-glass process [5] provides a patterned metal layer under the silicon substrate, both as an etch-stop layer and as a heat sink which prevents fabrication imperfection on the bottom of the silicon after Si DRIE. However, for Si-CMOS-MEMS devices, the metal layer etch stop cannot be adopted because the subsequent metal wet etch step will also etch the CMOS metal layers.

This paper demonstrates a Si-CMOS-MEMS process that enables fabricating thicker, high aspect-ratio structures compared to thin-film CMOS-MEMS devices. The Si-CMOS-MEMS process includes thick, high quality silicon under CMOS-MEMS structures to provide greater flexibility in designing integrated devices with higher performance without increasing the layout area. High aspect-ratio Si-CMOS-MEMS structures are created using back-side grinding on CMOS chips followed by chip bonding and front-side Si DRIE processes.

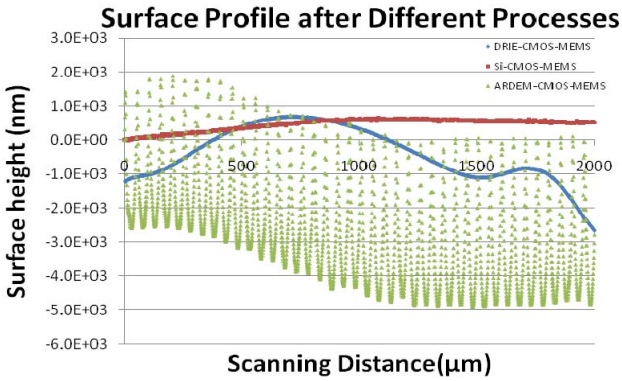


Figure 1 Back-side surface profile after different processes

Analysis of current state-of-the-art integrated processes

There are three main processes used for fabricating devices integrated with circuits: the post-CMOS process [1], the DRIE-CMOS-MEMS process [2-3], and the ARDEM-CMOS-MEMS process [4]. The strengths and weaknesses of these three different processes are analyzed and compared to demonstrate why the Si-CMOS-MEMS process is critical for achieving greater design flexibility.

Thin-film post-CMOS process [1]

When fabricating CMOS-MEMS devices which directly integrate with circuitry, the chip is exposed to oxide dry etching and the Si DRIE process, the top metal layer acting as a mask. After the underlying silicon is exposed, anisotropic etching is performed to create deep vertical trenches followed by isotropic etching to release the mechanical structure. The advantages of the post-CMOS process include compatibility with CMOS circuitry, high yield, and a simple post-process flow. The disadvantages include dimensional restrictions of mechanical components and a low temperature budget for other add-on processes.

DRIE-CMOS-MEMS process [2-3]

The DRIE-CMOS-MEMS process adopts back-side

photolithography and a DRIE process followed by the post-CMOS process where the front side metal layer acts as a mask. This process is mainly used to improve flatness and increase sensitivity by fabricating CMOS-MEMS devices which have Si underneath. However, the microloading effect and aspect ratio dependent etching (ARDE) cause up to 5 µm of non-uniformity of the back-side Si. The advantages of the DRIE-CMOS-MEMS process, like the post-CMOS process include compatibility with CMOS circuitry, high yield, and design flexibility in thickness. The disadvantages include non-uniform back-side silicon resulting from ARDE and complexity in the process compared with the CMOS-MEMS process.

ARDEM-CMOS-MEMS process [4]

The ARDEM-CMOS-MEMS process adopts the aspect-ratio dependent etching modulation (ARDEM) patterning method on back-side silicon followed by post-CMOS process where the front side metal layer acts as a mask. The ARDEM method can restrict the thickness variation of the back-side silicon within 5 µm. However, the thickness variation on back-side silicon can still cause variation in device performance, especially for inertial sensors. Another drawback of this process is the complexity of the process flow.

Table 1 Comparison table of different integrated processes

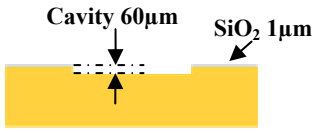
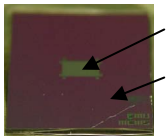
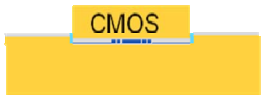
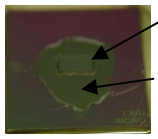
Comparing processes	Post-CMOS	DRIE-CMOS-MEMS	ARDEM-CMOS-MEMS
Back-side Si thickness(µm) after released	0	$0 < t < 50$ µm (upper limit based on minimum gap)	$0 < t < 50$ µm (upper limit based on minimum gap)
Aspect ratio	~5	~20	~20
Back-side Si uniformity	N/A	≤ 30 µm	≤ 5 µm
Process complexity	Low	Medium	Medium
Process cost	Low	Medium	Medium
Circuit integration	Y	Y	Y

Table 1 provides a summary of the above comparison between the three different integrated processes.

FABRICATION PROCESS AND PROCESS RESULTS

Table 2(f) shows the Si-CMOS-MEMS microstructures used for integrated sensors and electronics, which were formed using a silicon base and a thinned CMOS chip. Table 2 also illustrates the Si-CMOS-MEMS fabrication process and shows chip photos after each step. In step (a), a silicon carrier with a top cavity and 1 µm silicon dioxide layer on top was fabricated to hold the foundry CMOS chip. The depth of the top cavity provided a precise chip-height setting for the subsequent grinding step. In step (b), the CMOS chip was attached upside-down into the cavity using a unity polymer (UP) [6] as an adhesive. In step (c), the back-side of the chip was thinned down to 60 µm through a grinding and polishing process using various grit sandpapers.

Table 2 Si-CMOS-MEMS process fabrication steps and results

Process steps	Process Results
	
(a)	
	
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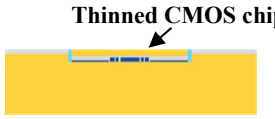	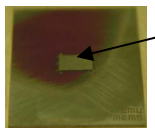
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	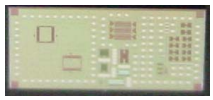
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	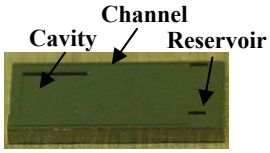
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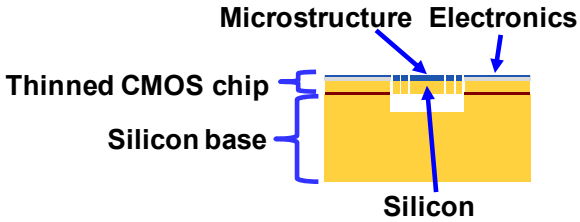
	
	
(f)	
	

The SiO_2 layer added in step (a) on the top of the carrier was used as a visual aid; its absence at the edges due to grinding indicated that the thickness of the chip is close to the desired value. The thinned chip was released from the carrier by decomposing the unity polymer at 250°C.

In step (d), another UP layer is painted on the back-side of the thinned CMOS chip. The back-side of the thinned chip was then attached to a custom silicon base over a device cavity using an epoxy bonding process. On the silicon base, transmitting channels and reservoirs were designed for capillary wicking of the epoxy. In step (e), the CMOS dielectric stack was etched directionally using CHF_3:O_2 reactive ion etching. In the final step (f), the CMOS silicon etching was performed through the thinned CMOS chip using the DRIE process with the bottom UP acting as an etch stop layer and a thermally conductive layer. Then, the UP layer was decomposed at 250°C to release the structures.

RESULTS AND DISCUSSION

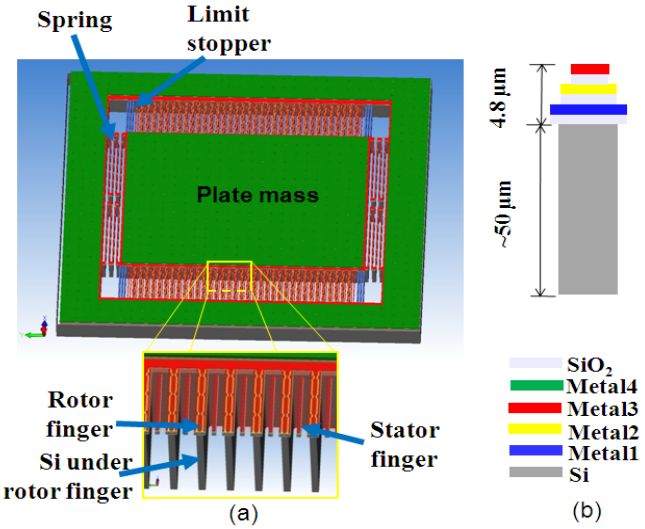


Figure 2 (a) 3D picture of a Si-CMOS-MEMS accelerometer (b) Cross-section diagram of the rotor finger

In Figure 2 (a), a 3D picture of the designed Si-CMOS-MEMS accelerometer is generated from emulation software, Coventorware 3D Memulator. The accelerometer includes a plate mass, serpentine springs, interdigitated capacitive fingers (rotor fingers and stator fingers) and limit stops. Using this Si-CMOS-MEMS process, additional silicon is included under the rotor fingers, spring structures and plate mass of the Si-CMOS-MEMS accelerometer.

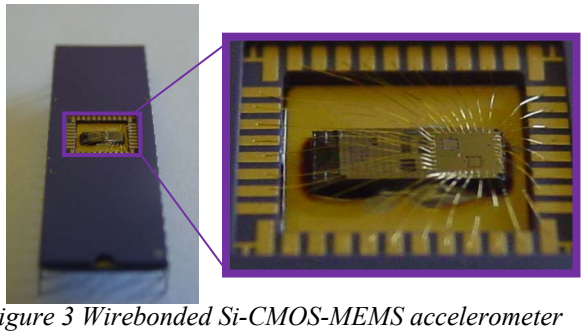


Figure 3 Wirebonded Si-CMOS-MEMS accelerometer

In Figure 3, two Si-CMOS-MEMS accelerometers integrated with on-chip circuitry are wirebonded in a 40 pin DIP package. The on-chip circuit design is similar to the electronics in a previously reported accelerometer design, [7] but with a higher modulation frequency of 10 MHz. Figure 4 illustrates the micrograph of the two accelerometers after the wirebond process. The two accelerometers are placed perpendicular to each other to sense two axes (x and y axes) acceleration. The surface of the chip after the decomposition of the unity polymer shows no contamination from the residue of unity polymer. However, there are some scratches present which were caused while the manipulating the chips during the process.

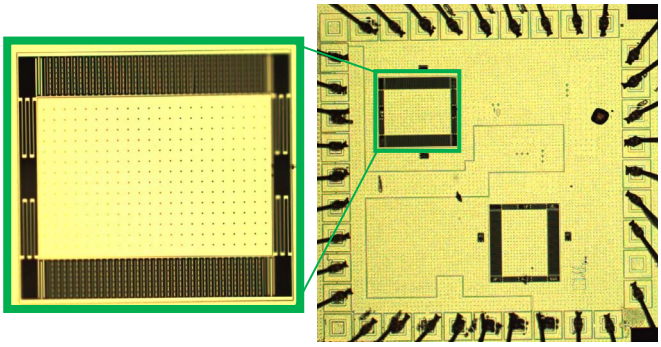


Figure 4 Micrographs of the Si-CMOS-MEMS accelerometer

Figure 5(a) shows SEM pictures of the fabricated Si-CMOS-MEMS accelerometer. The Si-CMOS-MEMS process successfully includes thick Si layers under the plate mass, springs and comb fingers. Figure 5(b) further illustrates the thickness of the silicon under the serpentine spring. However, a slight undercut in the silicon layer of the Si-CMOS-MEMS accelerometer is formed during the Si DRIE process due to ion deflection from the plasma and overheating [3].

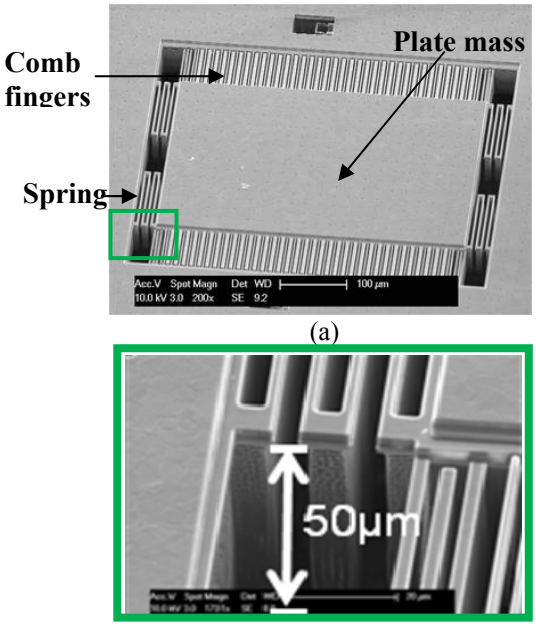
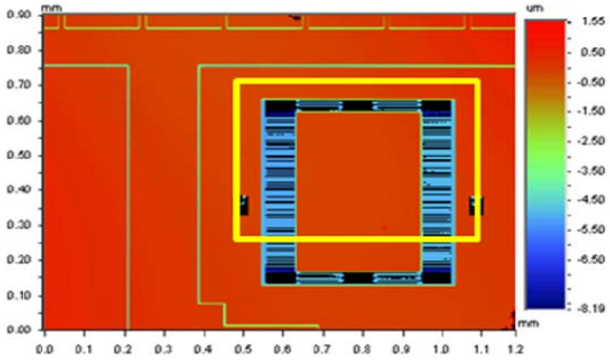


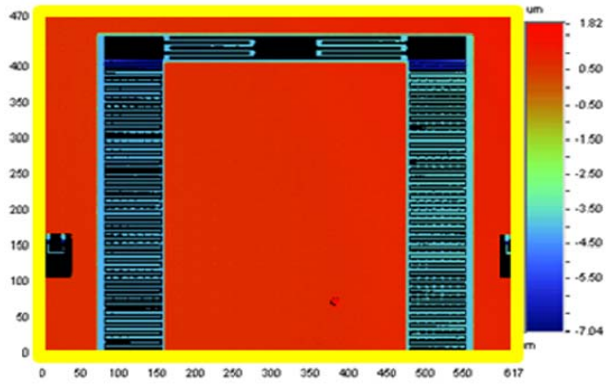
Figure 5 SEM pictures of Si-CMOS-MEMS accelerometer

This imperfection in the fabrication changes the effective spring constants of the serpentine springs, thereby effecting the sensitivity of the accelerometer.

The thick 50 µm silicon layer underneath the CMOS-MEMS accelerometers assures flatness of the devices. Figures 6(a) and 6(b) show white light profilometer pictures that illustrate the flatness of the device. The plate mass of the accelerometer includes CMOS interconnect layers up to the metal 4 layer. The deviation from a flat plane of over the whole accelerometer is less than 0.05 µm.



(a)



(b)

Figure 6 White light interferometer pictures of Si-CMOS-MEMS accelerometer

In Figure 6(a) and 6(b), the springs and comb fingers are all formed using metal 3 in the CMOS process. These features are also flat after release. The limit stops on each corner of the plate are slightly curled due to the complete undercut of the bottom silicon. This undercut is a result of the microloading effect of the large opening found next to the limit stops.

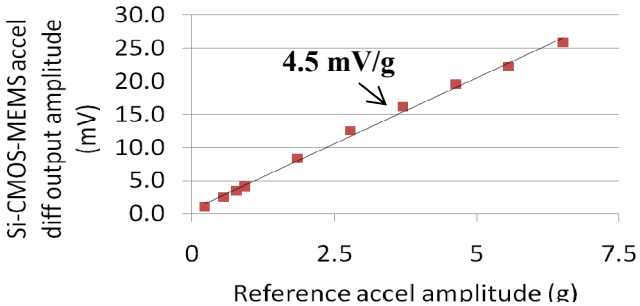


Figure 7. Sensitivity of the Si-CMOS-MEMS accelerometer

To demonstrate the functioning process, Figure 7 shows the sensitivity measured from the Si-CMOS-MEMS accelerometer. A shaker table with a calibrated accelerometer is used to test the accelerometer under various amplitudes of vibration [7]. The measured sensitivity is 4.5 mV/g.

CONCLUSION

The Si-CMOS-MEMS accelerometer fabricated in a 0.35 µm CMOS process successfully demonstrated the feasibility of the Si-CMOS-MEMS process. The process shows the superior profile of the back-side silicon when compared to other integrated processes using the post-CMOS process.

ACKNOWLEDGEMENT

The authors thank Suresh Santhanam and the staff at the Carnegie Mellon Nanofabrication Laboratory for assistance with the processing. This work is funded by the Defense Advanced Research Projects Agency under contract FA8650-08-1-7824.

REFERENCES

[1] G.K. Fedder, S. Santhanam, M. L. Reed, S. C. Eagle, D. F. Guillou, M. S.-C. Lu, and L. R. Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process," *Sensors & Actuators A*, vol. 57 (2), Nov. 1996, pp. 103-110.

[2] H. Xie, G.K. Fedder, Z. Pan and W. Frey,"Design and fabrication of an integrated CMOS-MEMS 3-axis accelerometer," in *Proc. of the 6th Int. Conf. on Modeling and Simulation of Microsystems Semiconductors, Sensors and Actuators (Nanotech '03),* San Francisco, CA, February 23-27, 2003, pp. 292-295.

[3] H. Qu and H. Xie,"Process development for CMOS-MEMS sensors with robust electrically isolated bulk silicon microstructures," *J. Micromech. Microeng.,* vol. 16, no. 5, pp. 1153-1161, Oct. 2007.

[4] P. J. Gilgunn and G.K. Fedder,"Flip-chip integrated SOI-CMOS-MEMS fabrication technology," in *Tech. Dig. of the Solid-State Sensors, Actuators and Microsystems Workshop*, Hilton Head Island, South Carolina, June 1-5, 2008, pp. 10-13.

[5] S. E. Alper, Y. Temiz, and T.Akin,"A compact angular rate sensor system using a fully decoupled silicon-on-glass MEMS gyroscope," *J. Microelectromechanical Systems*, vol.17, no. 6, Dec. 2008.

[6] http://www.promerus.com/

[7] A. Wung, R.V. Park, K.J. Rebello and G.K. Fedder, "Tri-axial high-g CMOS-MEMS capacitive accelerometer array", in *Proc. IEEE Int. Conf. on Micro Electro Mechanical Systems*, Jan. 13-17, 2008, pp.876–879.