Air-Gaps in 0.3 μm Electrical Interconnections

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***Abstract*—A copper/air-gap interconnection structure using a sacrificial polymer and SiO_2 in a damascene process has been demonstrated. The air-gap occupies the entire intralevel volume with fully densified SiO_2 as the planar interlevel dielectric. The copper was deposited by physical vapor deposition and planarized by chemical-mechanical planarization. The Ta/Cu barrier/seed layer was deposited by physical vapor deposition; the bulk copper was electrochemically deposited. The resulting structure has an effective intralevel dielectric constant of 2.19.**

***Index Terms*—Air-gaps, dielectric constant, interconnection, low-k.**

I. Introduction

THE NEED for low dielectric constant (low-k) materials for integrated circuits (IC's) originates from the shrinkage in the size of the transistor. Device shrinkage creates propagation delays, crosstalk noise, and power dissipation due to resistance-capacitance coupling [1]. In order to mitigate these problems, the National Technology Roadmap for Semiconductors has called for the qualification/preproduction of $k = 2.5$ to 2.0 starting in year 2000, and $k = 1.5$ to 2.0 in year 2003 [2]. Numerous approaches to achieving low-k materials are being pursued, including polymers, spin-on-glasses, and foams [3]. However, air-gaps provide the lowest effective dielectric constant available.

Multilevel interconnect structures have been fabricated in 0.3 μm structures [4] and evaluated using plasma deposited silicon dioxide [4], [5]. In this work, the air-gap occupies part of the region between the copper interconnections (intralevel air-gap structure). A greater fraction of the intralevel cavity was composed of air by use of a two-step process, using the controlled plasma assisted deposition of silicon dioxide [5]. In a different approach, sacrificial materials have been used as "placeholders" in the process sequence, so that the interlevel dielectric (dielectric material between metal levels) can be fabricated on a solid (although temporary) layer. Havemann has published an intralevel air-gap technology using a sacrificial place-holder and a porous overcoat (interlevel dielectric) [6]. The use of a porous layer imposes limitations to the materials set. Anand *et al.*have published an intralevel air-gap using carbon as the "place holder" sacrificial material [7]. After deposition of the overcoat interlevel dielectric, oxygen is allowed to permeate the overcoat and oxidize the carbon to carbon dioxide at 450 °C. In addition to the concern over oxygen at 450 °C affecting the metal and other materials, the rate of transport of oxygen and carbon dioxide, and the possibility of oxidation residues were not addressed.

In a previous work, we have demonstrated a material and process capable of forming air-gaps, although the demonstrations were on a larger size scale and IC compatible metallization was not used [8]. In this work, we demonstrate the first 0.3 μm air-gap process using a sacrificial polymer (processed and decomposed in an inert atmosphere) and a single damascence process flow.

II. Experimental

The sacrificial polymer used in this study was a copolymer of butylnorbornene and triethoxysilyl norbornene (Unity Sacrificial Polymer™, BFGoodrich, Cleveland, OH). Unity was dissolved as a 12 wt.% solution in mesitylene.

The air-gaps were prepared using 150 mm diameter silicon wafers. The wafers were spin coated with Unity at 3500 rpm for 30 s, which yielded a 1.3 μm thick layer. The film was soft baked at 120 °C for 3 min. A 500-nm thick layer of SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) at 200 °C, using a gas mixture of N_2O and SiH_4 diluted in N_2. A gap fill and planarization test structure for 0.3 μm interconnections was printed onto the SiO_2 layer using a DUV stepper. The photoresist pattern was transferred to the SiO_2 layer by reactive ion etching (RIE) in an Applied Materials P5000 etcher. The patterned SiO_2 layer served as the etch mask for reactive ion etching the Unity polymer using O_2 and CHF_2 in Ar at a pressure of 150 mtorr [9]. A blanket tantalum liner (50 nm) and blanket seed layer of copper (100 nm) were deposited onto the patterned Unity surface by physical vapor deposition in a Novellus M2i. The Ta was deposited at temperatures between 100 °C and 150 °C, while the copper was deposited at sub-ambient temperature. Following barrier/seed layer deposition, copper was electrochemically deposited by dc plating at constant current density on a Semitool Equinox platform using Enthone CuBath M. After copper deposition, the structure underwent chemical-mechanical planarization (CMP) using slight modifications to conventional damascene patterning of copper.

The CMP was performed using an IPEC-Planar (now Speedfam-IPEC) 372 M on Rodel IC 1400 pad. The downward pressure of the polish arm was 2.5 psi with 1.5 psi back pressure; the speed of the platen and carrier was 30 rpm; the slurry flow rate was 200 mL/min. A diluted (1 : 1 by vol.) Rodel metal slurry containing alumina particles and a proprietary liquid,

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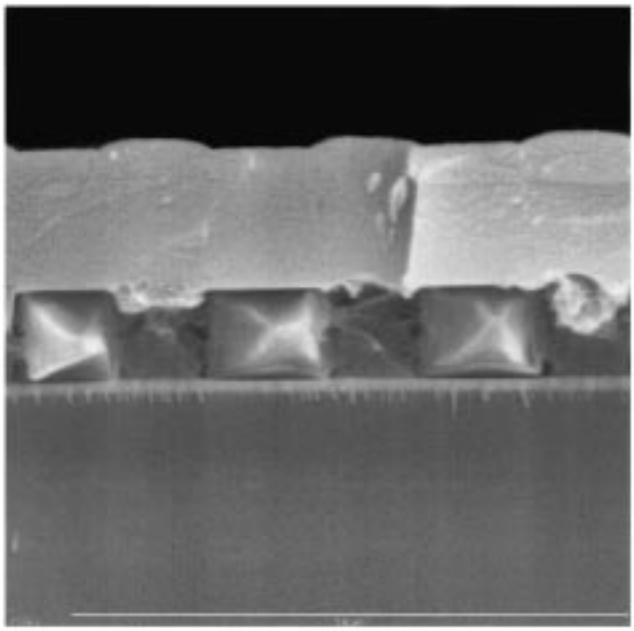


Fig. 1. Cross-sectional scanning electron micrograph of copper damascene structure. Three copper lines are shown separated by Unity polymer and overcoated with SiO_2. A 5 μm marker is shown on the bottom of the figure.

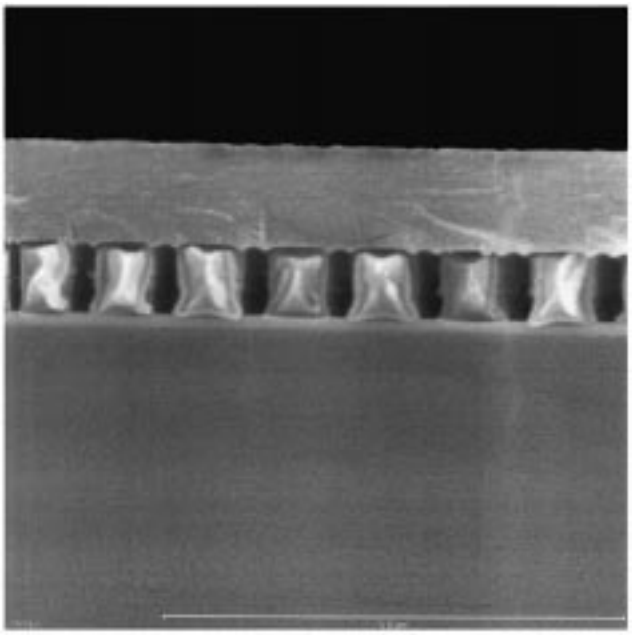


Fig. 2. Cross-sectional scanning electron micrograph of copper/air-gap structure. Seven copper lines are shown separated by air-gaps and overcoated with SiO_2. A 5 μm marker is shown on the bottom of the figure.

B00045, was used to remove copper, while a diluted (1 : 1 by vol.) Cabot colloidal silica slurry, SS25, was used to remove the tantalum liner. A tantalum liner is not usually removed with the KOH-based SS25 slurry in conventional damascene structure with oxide, since KOH-based slurry has a high removal rate for oxide [10]. However, the removal rate of Unity with this slurry was very low, <30 nm/min, as measured with blanket Unity films. Care was particularly taken to remove all metal from the top of the Unity polymer with minimal Unity erosion and scratching. After CMP, the wafers were cleaned by OnTrak DSS-200 double side brush scrubber with PVA brushes.

After CMP of copper, a 1.1 μm thick layer of SiO_2 was deposited by PECVD at 200 °C to form the overcoat dielectric. The hard mask used for patterning the sacrificial polymer could be removed by reactive ion etching or wet etching prior to PECVD deposition. The air-gaps were achieved by heat treatment at 425 °C for 2 h in a nitrogen purged furnace. During this process, the Unity decomposed and permeated through the SiO_2 overcoat dielectric leaving the gas cavity. The decomposition and removal rate of the sacrificial polymer was independent of pattern density.

The effective dielectric constant of the composite structure was calculated using Maxwell 2D Field Simulator (Ansoft Corp., Pittsburgh, PA). The dielectric constant could not be directly measured because the structures were built on silicon.

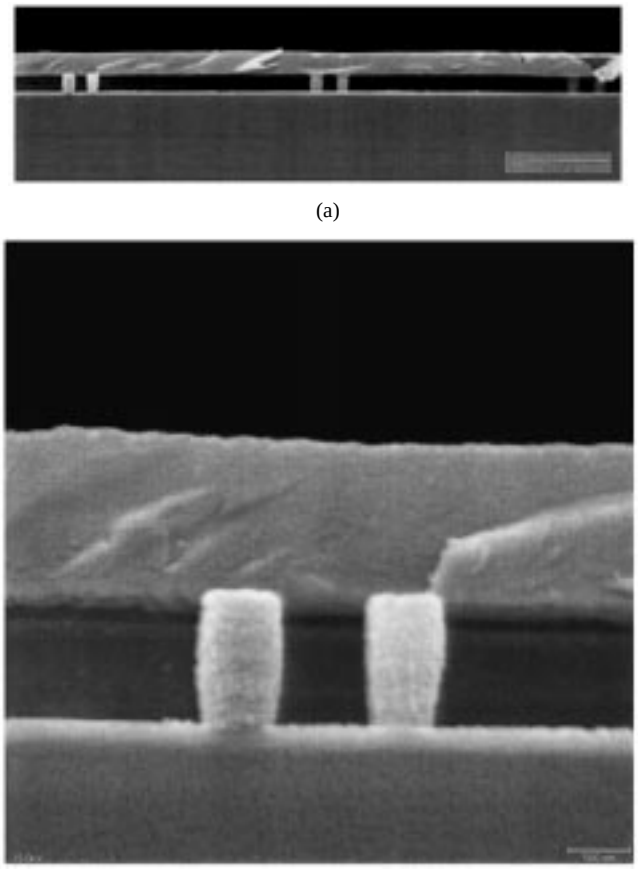
III. Results and Discussion

A damascene process flow was used to produce the copper/air-gap structure. A sacrificial polymer was used as the place-holder for fabrication of the interlevel dielectric (SiO_2). Fig. 1 shows a scanning electron micrograph (cross sectional view) of the 0.3 μm interconnection test structure with the Unity sacrificial polymer still in place (before polymer decomposition). The straight, vertical side walls of the copper are due to the anisotropic, reactive ion etching of the Unity polymer, which was the template for copper filling.

After deposition of the SiO_2 interlevel dielectric, the sample was heated to the decomposition temperature of the polymer. The gaseous products of the thermal decomposition permeated through the SiO_2 overcoat leaving the copper/air-gap structure shown in Fig. 2. The copper is 0.65 μm wide and 0.73 μm high. The air-gap between the copper lines is 0.26 μm wide. The copper/SiO_2 overcoat layer has very good planarity, as seen in Fig. 2. The Ta liner on the copper can be seen easily on the sides and bottom of the copper interconnections (Figs. 1 and 2). The sidewall shape of the copper seen in Fig. 1 is retained in Fig. 2. In multilayered metal/insulator structures with intralevel air-gaps, the sacrificial polymer can either be decomposed after each level or after more than one level has been fabricated. Both process sequences have been used. Decomposition after fabrication of multiple levels is preferred.

The effective intralevel dielectric constant between copper interconnections (0.73 μm high and 0.65 μm wide) with an air-gap (0.73 μm high and 0.29 μm wide) and 1.1 μm of SiO_2 ($e = 4.0$) above and below the copper was simulated using Maxwell 2D Field Simulator. The effective dielectric constant was calculated to be 2.19. Fringing fields in the SiO_2 (above and below the copper/air-gap interconnections) increase the effective dielectric constant above that of the air. If a lower dielectric constant overcoat dielectric were used, the effective dielectric constant of the composite would be reduced. For example, if the interlevel dielectric constant were 2.7 (as with some polymers or foams, rather than 4.0 for SiO_2), then the effective dielectric constant of the composite would be 1.71.

Fig. 3 shows a second test structure. This cross section shows copper lines separated by a 700 μm wide air-gap. The air-gaps between copper structures are much wider and the



(a)

(b)

Fig. 3. Cross-sectional scanning electron micrograph of copper/air-gap with wide gaps between the copper lines. (a) Lower magnification with a 5 μm marker shown. (b) Higher magnification with a 500-nm marker.

copper-to-air-gap ratio is much greater. The height of the Cu lines in Fig. 3 is 1.0 μm. The overcoat material is $\sim$1.1 μm thick PECVD deposited SiO_2. The planarity of the air-gap structures in Fig. 3 is very good. The reactive ion etching of Unity was highly anisotropic, which is advantageous for creation of high aspect ratio structures. The most significant advantages of the present method of fabrication of air-gaps over the all-PECVD oxide air-gap method [4]–[6] are the lack of oxide on the metal sidewalls as well as on the bottom of the air-cavity and the lack of protrusions of air-cavities into the top overcoat layer. Therefore, subsequent polishing steps are more robust, with additional flexibility in the overcoat layer thickness. The critical aspects of the Unity Sacrificial Polymer™ in this process are

1) its high glass transition temperature allowing dimensional stability during processing;
2) its slow decompostion rate mitigating problems of pressure build-up during air-gap formation;
3) residue-free nature of the cavities due to the completeness of the decomposition;
4) temperature of the decomposition allowing other processing steps to be carried out before formation of the cavities [11].

IV. Conclusion

We have demonstrated the feasibility of fabrication of metal/air-gap structures of very small dimensions, of the order of few hundreds of nanometers in width by using a sacrificial polymer. Significantly, the lack of oxide on the sidewalls of the metal and on the bottom of the air-cavities and the lack of protrusion of air-cavities into the top overcoat layer are important for this application. The incorporation of such air-gaps between the metal conductors in integrated circuits is expected to reduce the intralevel dielectric constant significantly, thereby reducing the RC delays and crosstalk in ICs.

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