

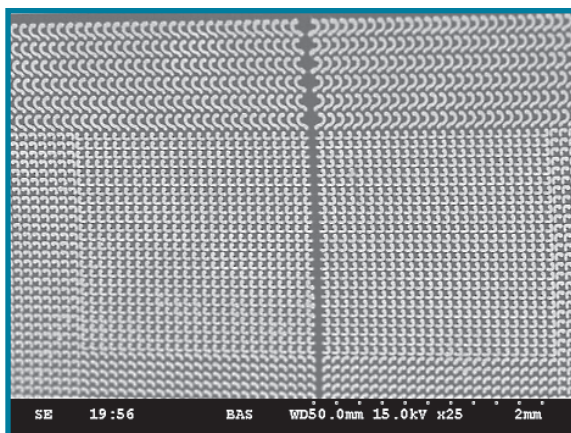
SoL-Compliant Wafer-Level Package Technologies

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A key component of the interconnection hierarchy that will be severely challenged by gigascale integration (GSI) is chip-to-module interconnection integrating a packaged chip into a digital system.¹ A gigascale system-on-a-chip (GSoC) calls for the development of new and cost-effective integrated I/O interconnect solutions using, for example, integrated electrical, optical and rf approaches to meet all the I/O requirements of the sub-50 nm International Technology Roadmap for Semiconductors technology nodes.² Meeting these challenges is essential for the semiconductor industry to transcend known limits on interconnects that would otherwise decelerate or halt the historical rate of progress toward GSI.

In general, power, clock and signal I/O functions will be met by the selective integration of fine-pitch (<30 μm pitch area array) electrical, optical and rf I/O interconnect technologies. These high-density integrated I/O interconnects will be especially important for novel 3-D structures as well as high-current (>400 A) and high-bandwidth (>40 Tb/sec) applications.¹ To investigate the above issues, focus must be given to overcoming long-range and fundamental barriers in chip-to-module interconnects by advancing fine-pitch compliant electrical, optoelectronic and rf in-



1. SEM showing part of an SoL package with 12×10^3 X-Y-Z-compliant chip I/O interconnects distributed across a cm^2 . In-plane compliance compensates for the CTE mismatch between the chip and the substrate. Out-of-plane compliance is needed during wafer-level testing/burn-in due to non-planarity of testing boards.

terconnections, as well as wafer-level testing and burn-in.

SoL packaging

Sea of leads (SoL) is a novel ultrahigh-density packaging technology designed to meet future chip-to-module interconnection needs. Unlike conventional packaging, SoL extends wafer-level batch fabrication of multilevel interconnect networks to include the chip's I/O leads. A SEM micrograph illustrates a portion of an SoL package with 12×10^3 X-Y-Z-compliant leads/ cm^2 (Fig. 1).³ In-plane and out-of-plane compliance were measured to be >30 μm . While the leads are X-Y-Z axis-compliant, they are short in length

and thus exhibit minimal parasitics from dc to 45 GHz. The calculated resistance and inductance of the leads are <25 m Ω and 0.1 nH, respectively.³ Low electrical parasitics are desirable at both low and high frequencies for efficient conductive coupling of power, low power dissipation in the leads and thus low heat generation by the package. The microwave characteristics of SoL were measured at wafer level using a two-port network analyzer with 150 μm coplanar ground-signal-ground (GSG) probes.

To characterize the compliant interconnects, 15- μm -thick Au leads were fabricated on a 15- μm -thick polymer film. The return-loss and insertion-loss of the GSG lead interconnection were measured to be <20 and 0.2 dB, respectively, at 45 GHz.¹ In comparison, for example, insertion-losses before and after the addition of underfill within a flip-chip package mounted on an alumina substrate with $75 \times 150 \mu\text{m}$ bumps interconnected by 600- μm -long

At a Glance

Sea of leads (SoL), a novel ultrahigh-density packaging technology designed to meet future chip-to-module interconnection needs, enhances the manufacturing cycle's tail-end-of-line phase by driving down cost and increasing testing efficiency.

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50 Ω coplanar waveguides were 0.6 and 1.8 dB, respectively, at 40 GHz.⁴ The normalized impedance of the load as seen by the microwave probes was derived and plotted on a Smith chart. At low frequencies (up to a few gigahertz), the leads appear as shorts.

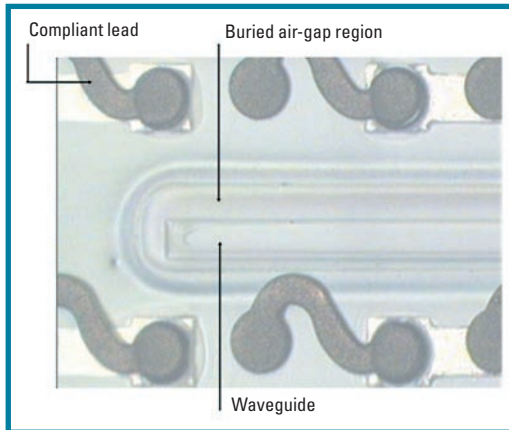
Another microwave measurement was made on a fully processed package where the leads were connected in pairs by 100 and 1 μm -thick copper interconnects routed along the wafer surface. The worst case return-loss and insertion-loss for a pair of inter-connected leads were measured to be <12 and 1.2 dB, respectively. These measurements include the losses due to the Cu interconnects. Crosstalk between adjacent parallel leads was <30 dB at 45 GHz, and crosstalk between orthogonal leads was \sim 40 dB. All interconnect structures were \sim 20 μm wide. All the compliant leads measured were \sim 110 μm long.

Similar microwave measurements for other packaging technologies have been done. It appears that the SoL measurements reported above compare well to flip-chip packages, widely used in microwave applications. However, the ultrahigh I/O density of SoL can provide an exceptionally high I/O bandwidth that would be difficult to match using alternate packaging technologies. For example, if 8000 leads are assigned as signal I/Os and operated at only 5 GHz, the SoL package shown in Figure 1 can yield an aggregate electrical I/O bandwidth of 40 Tb/($\text{cm}^2\text{-sec}$). Also, an SoL package avoids microwave performance degradation caused by underfill, since no underfill is required during assembly. This is in contrast to assembly requirements of flip-chip and BGA packages, where the presence of underfill increases insertion-loss and shifts the return-loss frequency response to lower frequencies.^{4,5}

An important aspect of SoL is the set of performance enhancements it offers a mixed-signal SoC.¹ SoL can enhance the dc power distribution as well as satisfy 3-D structure I/O requirements. Because SoL processing requires low temperature (<250°C), it is expected that WLP processing will not damage previously fabricated structures during front- and back-end-of-line processing.^{3,6}

Optical interconnects

Next-generation SoL technology will incorporate optical waveguide interconnection to permit global optical clock distribution within high-performance chips.



2. Micrograph of an embedded optical waveguide and air-gap region within an SoL package.

Optical waveguide interconnection allows for planar packaging of a hybrid electrical/optical system in a manner conducive to future heat removal and power supply requirements. In addition, polymer waveguide technologies offer immediate and low-cost compatibility with wafer-level fabrication processes. Minimal redesign of the global distribution would be required with increases in clock frequency, since design of the cross-sectional dimensions of an optical waveguide is independent of the clock frequency. Global propagation of the local clock frequency would be possible, thereby eliminating the need for global clock repeaters. This also permits the removal of cycle-to-cycle jitter from the global clock signal in its delivery to optoelectronic receivers for optical-to-electrical conversion. Finally, optical waveguide clock distribution would allow for enhanced predictability with respect to the arrival time of clock pulses at different optoelectronic receivers, thereby eliminating unexpected components of global distribution skew.⁷

A key feature of the proposed technology is the use of embedded air-gap regions as the upper cladding for optical waveguides. Embedded air-gap cladding regions allow for a maximization in refractive index contrast, n , between waveguide core and cladding, and hence per-

mit smaller bending radii and higher waveguide densities due to tighter confinement within the waveguide core. By placing optical waveguides within the package, via blockage concerns are eliminated with respect to waveguide routing, leaving only electrical I/O interconnection to obstruct intra-chip waveguide routing.

The portion of the fabrication process associated with optical waveguide integration begins following the definition of bond pad regions for compliant interconnection. In recent experiments, optical-quality SiO_2 serves as the lower cladding region of optical waveguides (although this is not a requirement). Following deposition and curing of the waveguide material (which consists of an alkoxy-siloxane epoxy⁸ obtained from Polyset Inc.), channel waveguide regions are defined. To create the embedded air-gap cladding regions, a sacrificial photosensitive polymer composite (Unity 200) is applied and patterned. An overcoat polymer is then applied to embed the air gap and waveguide regions, where, upon thermal cure, the remaining polymer regions decompose to leave an embedded air gap. Figure 2 is a micrograph of a single waveguide from an SoL package with 1000 electrical I/Os/ cm^2 and 32 optical waveguides, where individual compliant leads, an optical waveguide, and a buried air-gap region are shown. By incorporating a buried air gap, an $n=0.52$ is achieved between core and upper cladding regions. Beam propagation methods reveal that, by incorporating an air-gap cladding region, the minimum allowed edge-to-edge spacing between adjacent waveguides is reduced by more than three times.⁹

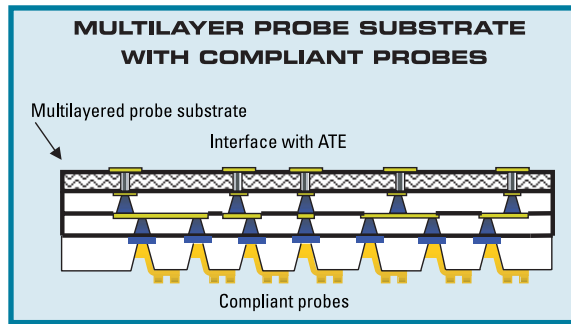
Testability benefits

Ultrahigh-I/O-density SoL technology has the potential to revolutionize testability of future GSoCs. Because the die are still in wafer form after packaging, it becomes possible to test multiple packaged die. Multi-die site testing is the first step toward wafer-level test and burn-in. The test time per wafer in multi-die site testing is reduced since the mechanical stepping probe head requires fewer steps to cover an entire wafer. Shorter test time per wafer translates to reduced test costs.

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Two key aspects of testing an integrated circuit are controllability and observability.¹⁰ Today, test vectors are generated from complex algorithms and applied using test application methods such as boundary scan and built-in self-test.^{2,10} These methods are designed to be "pin-stingy," since only a very small number of I/O pins on a package are devoted to testing. Test designers have to ensure not only that the targeted faults are activated but also that the effects of those faults are propagated to at least one of the few observable outputs. The SoL package will allow designers to devote a large number of I/Os to testing, in some cases even more than the total number of I/Os on some of today's packages. The high I/O density provides access to previously unreachable nodes on a chip — increasing the ability to control what (test) signals are entering the system, and to observe the response to those stimuli. Moreover, the availability of a larger number of I/O pins for testing creates room for development of new, more efficient test procedures. For example, the high I/O density of the SoL package could be used for the physical partitioning of a GSoC into individual cores. Each core could then be pseudo-exhaustively tested, individually or in parallel. Breaking up the device-under-test (DUT) into smaller units would reduce the volume of generated test patterns, while still maintaining high test fault coverage.

The benefits of ultrahigh-density WLP technology in terms of testing can be realized only with use of a compatible probe substrate to interface the SoL DUT with external test equipment. A novel high-density compliant probe technology has been conceived to achieve this task. The probes can be batch-fabricated for use in various probe card configurations to provide a reliable and high-speed interface between high-pin-count packages on one side and test equipment on the other side.¹¹ A schematic of a simple multilayered probe substrate is shown in Figure 3. The compliant probes themselves are a modification of the leads from the current SoL process, and are designed to provide compliance in the X, Y and Z directions. A SEM micrograph of a single



3. Schematic of a multilayer probe substrate with compliant probes.



4. SEM of a single compliant probe consisting of an "S"-shaped lead, and four prism-shaped metal probe tips. Thousands of probes like this one can be fabricated simultaneously on the probe substrate.

compliant probe is shown in Figure 4. The structure consists of an S-shaped lead connected to the substrate through a via on one end and terminated by a circular contact at the other. On top of the circular contact lie four raised prism-shaped contacts with which the solder bumps of the package under test would come in contact. The lead rests on a compliant interposer that has been shown to provide compliance along all three axes.³

When a compliant package is to be probed, it provides further flexibility for better contact. The probes provide all the requisite compliance while contacting a non-compliant package. As the compliant probes are a progeny of the SoL leads, they inherit their high-density, high-bandwidth and low-parasitic characteristics. The compliant probes are fabricated in an area array to match the footprint of the SoL package. This technique can easily be extended to probe multiple die sites of not only WLPs, but of other high-density packages as well.

The use of SoL enhances the tail-end-of-line phase of manufacturing not only by driving down cost, but by increasing the efficiency of testing a GSoC. The compliant probe substrate extends the benefits of SoL by providing a reliable in-

terface between the DUT and the ATE. Probe substrates fit with these high-density, batch-fabricated compliant probes facilitate the first steps toward massively parallel test methods and achieving full wafer contact and test capabilities. •

References

1. M.S. Bakir, et al, "Sea of Leads Characterization and Design for Compatibility for Board Level Optical Waveguide Interconnection," to be presented, IEEE Custom Integrated Circuits Conference, Orlando, Fla., May 2002.
2. 2001 International Technology Roadmap for Semiconductors (ITRS), SIA.
3. M.S. Bakir, et al, "Sea of Leads Ultra-High-Density Compliant WLP Technology," to be presented, 52nd Electronics and Components Technology Conf., San Diego, May 2002.
4. Z. Feng, et al, "RF and Mechanical Characterization of Flip-Chip Interconnects in CPW Circuits with Underfill," *IEEE Trans. on Microwave Theory and Techniques*, December 1998, p. 2269.
5. H. Kusamitsu, et al, "The Flip-Chip Bump Interconnection for Millimeter-Wave GaAs MMIC," *IEEE Trans. Electron. Packaging Manuf.*, January 1999, p. 23.
6. H.A. Reed, et al, "Fabrication of Microchannels Using Polycarbonates as Sacrificial Materials," *Journal of Micromechanics and Microengineering*, October 2001, p. 733.
7. P.J. Restle, et al, "A Clock Distribution Network for Microprocessors," *IEEE J. Solid State Circuits*, May 2001, p. 792.
8. A. Jain, et al, "Porous Silica Materials as Low-k Dielectrics for Electronic and Optical Interconnects," *Thin Solid Films*, Vol. 398-399, 2001, p. 513.
9. A.V. Mulé, et al, "Input Coupling and Guided-Wave Distribution Scheme for Board-Level Intra-Chip Optical Clock Distribution Network Using Volume Grating Coupler Technology," *Proc. IEEE International Interconnect Technology Conf.*, San Francisco, June 2001, p. 128.
10. M.L. Bushnell and V.D. Agrawal, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers (Boston, 2000).
11. H.D. Thacker, et al, "Compliant Probe Substrates for Testing High Pin-Count Chip Scale Packages," to be presented, 52nd Electronics and Components Technology Conf., San Diego, May 2002.

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