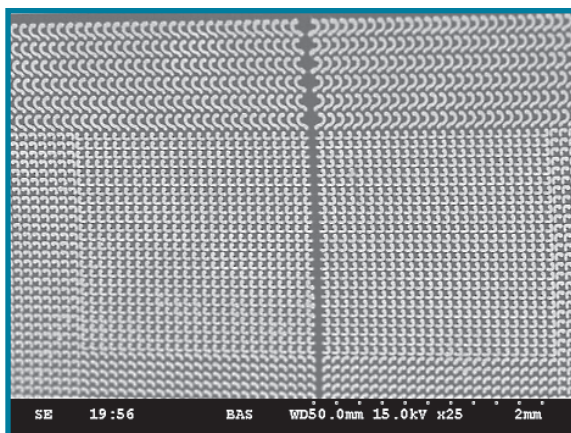# SoL-Compliant
Wafer-Level Package
Technologies

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A key component of the interconnection hierarchy that will be severely challenged by gigascale integration (GSI) is chip-to-module interconnection integrating a packaged chip into a digital system.[1] A gigascale system-on-a-chip (GSoC) calls for the development of new and cost-effective integrated I/O interconnect solutions using, for example, integrated electrical, optical and rf approaches to meet all the I/O requirements of the sub-50 nm International Technology Roadmap for Semiconductors technology nodes.[2] Meeting these challenges is essential for the semiconductor industry to transcend known limits on interconnects that would otherwise decelerate or halt the historical rate of progress toward GSI.

In general, power, clock and signal I/O functions will be met by the selective integration of fine-pitch (<30 µm pitch area array) electrical, optical and rf I/O interconnect technologies. These high-density integrated I/O interconnects will be especially important for novel 3-D structures as well as high-current (>400 A) and high-bandwidth (>40 Tb/sec) applications.[1] To investigate the above issues, focus must be given to overcoming long-range and fundamental barriers in chip-to-module interconnects by advancing fine-pitch compliant electrical, optoelectronic and rf in-

1. SEM showing part of an SoL package with 12×10^3 X-Y-Z-compliant chip I/O interconnects distributed across a cm². In-plane compliance compensates for the CTE mismatch between the chip and the substrate. Out-of-plane compliance is needed during wafer-level testing/burn-in due to non-planarity of testing boards.

terconnections, as well as wafer-level testing and burn-in.

SoL packaging

Sea of leads (SoL) is a novel ultrahigh-density packaging technology designed to meet future chip-to-module interconnection needs. Unlike conventional packaging, SoL extends wafer-level batch fabrication of multilevel interconnect networks to include the chip's I/O leads. A SEM micrograph illustrates a portion of an SoL package with 12×10^3 X-Y-Z-compliant leads/cm² (Fig. 1).[3] In-plane and out-of-plane compliance were measured to be >30 µm. While the leads are X-Y-Z axis-compliant, they are short in length

and thus exhibit minimal parasitics from dc to 45 GHz. The calculated resistance and inductance of the leads are <25 mΩ and 0.1 nH, respectively.[3] Low electrical parasitics are desirable at both low and high frequencies for efficient conductive coupling of power, low power dissipation in the leads and thus low heat generation by the package. The microwave characteristics of SoL were measured at wafer level using a two-port network analyzer with 150 µm coplanar ground-signal-ground (GSG) probes.

To characterize the compliant interconnects, 15-µm-thick Au leads were fabricated on a 15-µm-thick polymer film. The return-loss and insertion-loss of the GSG lead interconnection were measured to be <20 and 0.2 dB, respectively, at 45 GHz.[1] In comparison, for example, insertion-losses before and after the addition of underfill within a flip-chip package mounted on an alumina substrate with 75×150 µm bumps interconnected by 600-µm-long

At a Glance

Sea of leads (SoL), a novel ultrahigh-density packaging technology designed to meet future chip-to-module interconnection needs, enhances the manufacturing cycle's tail-end-of-line phase by driving down cost and increasing testing efficiency.

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50Ω coplanar waveguides were 0.6 and 1.8 dB, respectively, at 40 GHz.[4] The normalized impedance of the load as seen by the microwave probes was derived and plotted on a Smith chart. At low frequencies (up to a few gigahertz), the leads appear as shorts.

Another microwave measurement was made on a fully processed package where the leads were connected in pairs by 100 and 1 µm-thick copper interconnects routed along the wafer surface. The worst case return-loss and insertion-loss for a pair of interconnected leads were measured to be <12 and 1.2 dB, respectively. These measurements include the losses due to the Cu interconnects. Crosstalk between adjacent parallel leads was <30 dB at 45 GHz, and crosstalk between orthogonal leads was ~40 dB. All interconnect structures were ~20 µm wide. All the compliant leads measured were ~110 µm long.

Similar microwave measurements for other packaging technologies have been done. It appears that the SoL measurements reported above compare well to flip-chip packages, widely used in microwave applications. However, the ultrahigh I/O density of SoL can provide an exceptionally high I/O bandwidth that would be difficult to match using alternate packaging technologies. For example, if 8000 leads are assigned as signal I/Os and operated at only 5 GHz, the SoL package shown in Figure 1 can yield an aggregate electrical I/O bandwidth of 40 Tb/(cm²-sec). Also, an SoL package avoids microwave performance degradation caused by underfill, since no underfill is required during assembly. This is in contrast to assembly requirements of flip-chip and BGA packages, where the presence of underfill increases insertion-loss and shifts the return-loss frequency response to lower frequencies.[4,5]

An important aspect of SoL is the set of performance enhancements it offers a mixed-signal SoC.[1] SoL can enhance the dc power distribution as well as satisfy 3-D structure I/O requirements. Because SoL processing requires low temperature (<250°C), it is expected that WLP processing will not damage previously fabricated structures during front- and back-end-of-line processing.[3,6]

Optical interconnects

Next-generation SoL technology will incorporate optical waveguide interconnection to permit global optical clock distribution within high-performance chips.
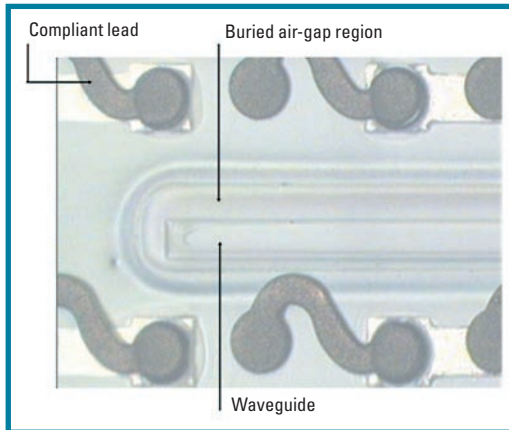
2. Micrograph of an embedded optical waveguide and air-gap region within an SoL package.

Optical waveguide interconnection allows for planar packaging of a hybrid electrical/optical system in a manner conducive to future heat removal and power supply requirements. In addition, polymer waveguide technologies offer immediate and low-cost compatibility with wafer-level fabrication processes. Minimal redesign of the global distribution would be required with increases in clock frequency, since design of the cross-sectional dimensions of an optical waveguide is independent of the clock frequency. Global propagation of the local clock frequency would be possible, thereby eliminating the need for global clock repeaters. This also permits the removal of cycle-to-cycle jitter from the global clock signal in its delivery to optoelectronic receivers for optical-to-electrical conversion. Finally, optical waveguide clock distribution would allow for enhanced predictability with respect to the arrival time of clock pulses at different optoelectronic receivers, thereby eliminating unexpected components of global distribution skew.[7]

A key feature of the proposed technology is the use of embedded air-gap regions as the upper cladding for optical waveguides. Embedded air-gap cladding regions allow for a maximization in refractive index contrast, n, between waveguide core and cladding, and hence permit smaller bending radii and higher waveguide densities due to tighter confinement within the waveguide core. By placing optical waveguides within the package, via blockage concerns are eliminated with respect to waveguide routing, leaving only electrical I/O interconnection to obstruct intra-chip waveguide routing.

The portion of the fabrication process associated with optical waveguide integration begins following the definition of bond pad regions for compliant interconnection. In recent experiments, optical-quality SiO_2 serves as the lower cladding region of optical waveguides (although this is not a requirement). Following deposition and curing of the waveguide material (which consists of an alkoxy-siloxane epoxy[8] obtained from Polyset Inc.), channel waveguide regions are defined. To create the embedded air-gap cladding regions, a sacrificial photosensitive polymer composite (Unity 200) is applied and patterned. An overcoat polymer is then applied to embed the air gap and waveguide regions, where, upon thermal cure, the remaining polymer regions decompose to leave an embedded air gap. Figure 2 is a micrograph of a single waveguide from an SoL package with 1000 electrical I/Os/cm² and 32 optical waveguides, where individual compliant leads, an optical waveguide, and a buried air-gap region are shown. By incorporating a buried air gap, an n=0.52 is achieved between core and upper cladding regions. Beam propagation methods reveal that, by incorporating an air-gap cladding region, the minimum allowed edge-to-edge spacing between adjacent waveguides is reduced by more than three times.[9]
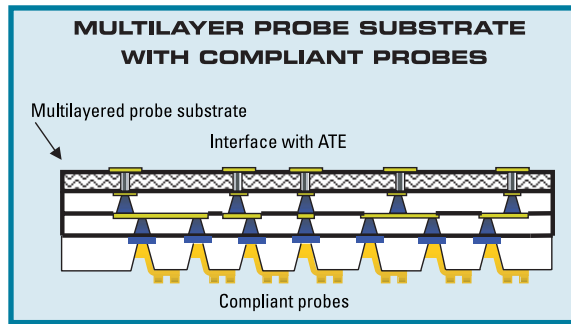
Testability benefits

Ultrahigh-I/O-density SoL technology has the potential to revolutionize testability of future GSoCs. Because the die are still in wafer form after packaging, it becomes possible to test multiple packaged die. Multi-die site testing is the first step toward wafer-level test and burn-in. The test time per wafer in multi-die site testing is reduced since the mechanical stepping probe head requires fewer steps to cover an entire wafer. Shorter test time per wafer translates to reduced test costs.